

PAVAN KENDAGANNA SWAMY

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EDUCATION

Master of Science in Computer Engineering Arizona State University, Tempe, AZ	May 2023
	GPA: 3.53/4

Relevant Coursework: Digital Systems Circuits, VLSI Design, Constructionist Approach to Microprocessor, Logic Design using System Verilog, Python, Computer Architecture-2, Foundation of Algorithms, Random Signal Theory.

Bachelor of Science in Electronics and Communication Engineering Sri Jayachamarajendra College of Engineering, Mysore, KA, India	May 2017
	GPA: 8.61/10

TECHNICAL SKILLS

Tools: Innovus, Cerebrus, Tempus, Genus, Harmony, RTL to GDSII, ICC2, Star RC, STA, Virtuoso, Spectre, Vivado.

Design: RTL Design, Layout Design, Logic Design, DRC, LVS, Pex.

Physical Design: ASIC, Synthesis, Floorplan, Delay, Power, Interconnect, Place and Route, Static Timing Analysis, and Clock Tree Synthesis.

Programming Languages: C, Python, Tcl(Beginner), Shell(Beginner); **Hardware Description Language:** Verilog/System Verilog.

PROFESSIONAL EXPERIENCE

Product Engineer Intern, Cadence Design Systems San Jose, California, USA	May 2022 – Dec 2022
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- Implemented full-flow physical design (PnR to signoff) and performed comprehensive timing analysis, using Innovus. Successfully optimized critical timing paths and achieved a 30% improvement in timing.
- Optimized leakage power on a design based on meticulous analysis of QoR and the cost. Accomplished 15% better leakage power at sign-off, while effectively managing a trade-off of 3.4% utilization.
- Employed Cerebrus to auto-configure the primitives and cost function, driving substantial improvements toward the desired objective. Leveraging Cerebrus, I achieved significant enhancement in QoR.
- Enhanced leakage power on an RTL synthesizable 16nm design using Genus. Achieved 18% better performance.
- Contributed essential support to the DSG team, assisting with debugging and verification of Innovus features.

Executive Engineer, Continental Automotive Components Pvt Ltd Bengaluru, India	July 2017 – July 2021
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- Developed driver-level software for projects according to customer requirements for DEM and FIM components to realize functionalities of the Advanced Driver Assistance System (ADAS).
- Identified possible bugs in software while testing and proposed feasible solutions.
- Analyzed customer issues and solved them on time which enhanced my technical credibility.
- Trained two new developers for the project, and created training materials about development, and testing procedures.

ACADEMIC PROJECTS

Design and synthesis of 2-bit Full Adder APR and post-APR, DRC, and LVS for ASAP 7nm PDK, ASU	Spring 2022
<ul style="list-style-type: none">Developed Verilog code for the design and synthesized netlist using Design Compiler.Performed APR using Innovus and imported GDS from Innovus into cadence virtuoso layout.Performed simulation using the Hspice simulator.	

Design and synthesis of AOI22, DRC, LVS, and pex for ASAP 7nm PDK, ASU	Spring 2022
<ul style="list-style-type: none">Designed AOI21 schematics and layout using Cadence Virtuoso.Devised test bench to observe delay and functionality by HSPICE simulation. Performed LVS, DRC, and Pex extraction.Compared the delay metrics of pre and post-layout simulation to understand the impact of RC delay.Placed the cells in a 3x3 matrix and cleared DRC to realize the importance of compact layout design.	

Design of 16x16 Register File with 1 write and 1 Read Port, ASU	Spring 2022
<ul style="list-style-type: none">Designed the schematic and layout of a 16x1 Column of the RF and of 4x16 Decoder.Integrated 16x1 Column Group with 4x16 Decoder to obtain 16x16 RF.Verified RF functionality with test scripts.	

Simulation and layout design of CMOS digital circuits using Virtuoso (Cadence), ASU	Fall 2021
<ul style="list-style-type: none">Simulated the various basic circuits and thoroughly analyzed their delay, rise, and fall times under various constraints.Designed a 4-bit adder with 32nm technology achieving an area of $33.26 \mu\text{m}^2$, a delay of 62.1pS.Implemented layout of digital circuits, designing a test bench and simulation using Hspice.	